Low & High Temperature SOI CMOS

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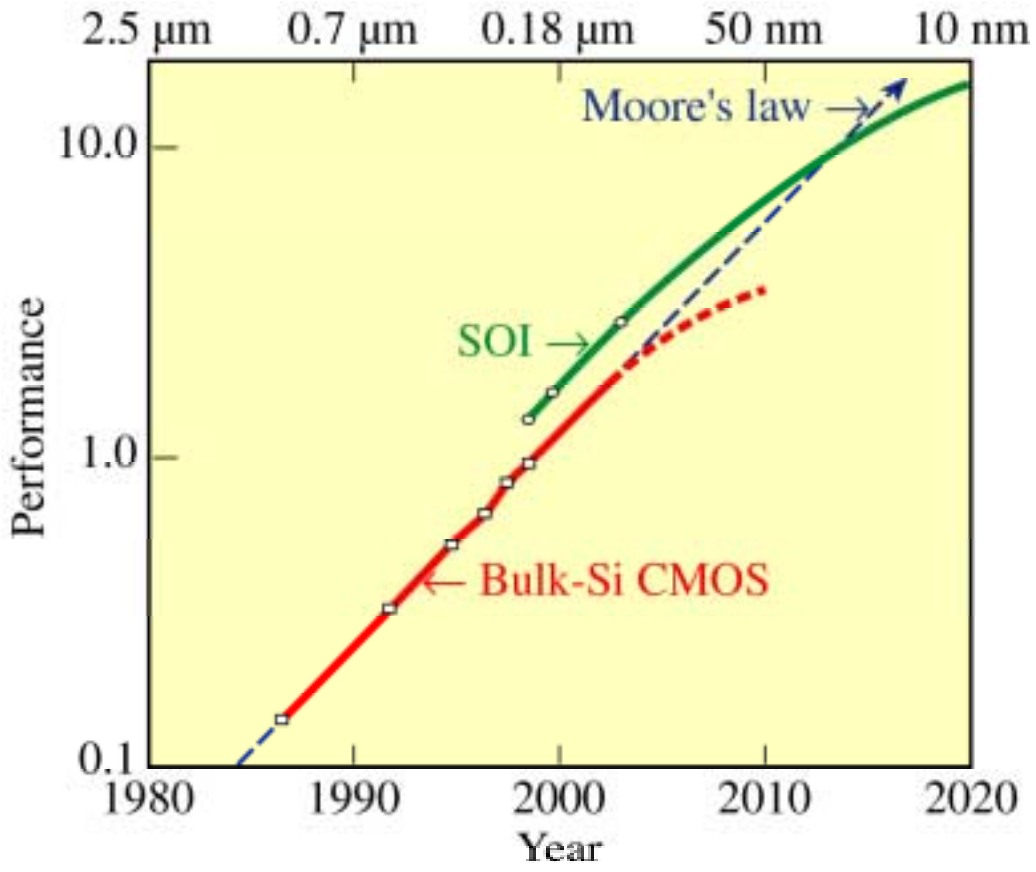
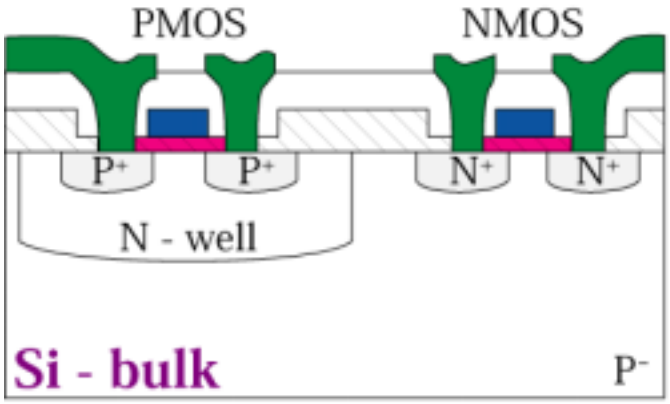
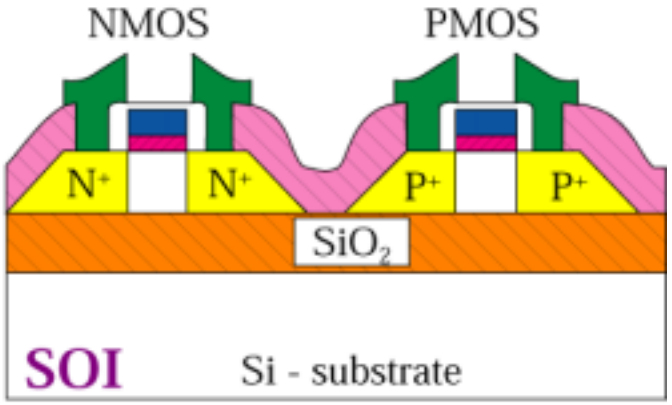
- **Context of SOI technology**
  - **Scalability issues**
  - **Trends in materials and devices**
- **SOI MOSFETs at low temperature**
  - **Properties and special mechanisms**
  - **Short-channel effects and reliability issues**
- **SOI MOSFETs at high temperature**
  - **Key parameters and mechanisms**
- **Innovating SOI devices**
  - **Extremely thin SOI MOSFETs**
  - **Double-Gate and 4-Gate MOSFETs**

Moore's Law & SOI



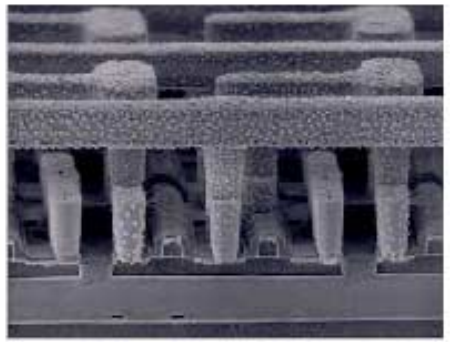
Why SOI ?





Dielectric isolation: vertical and lateral (no latch-up)
Vertical junctions: reduced leakage and capacitance
Excellent tolerance of transient radiation effects
Simpler processing & high flexibility: no wells or trenches
Ideal structure for sensors, MEMS, high-temperature devices

Attenuated short-channel effects: enhanced scaling
Low-voltage & low-power operation:
sharp subthreshold swing, reduced leakage, low V_T



Strategic Move to SOI

- High performance µP:

  IBM, Compaq, Motorola, HP, OKI, Samsung

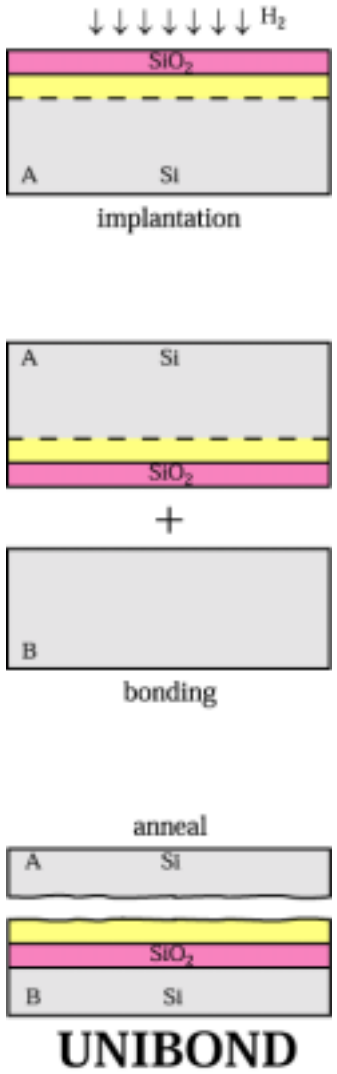
- Low-Power/Low-Voltage: Epson, Melco, TI
- Other markets: G3 portable phones, optoelectronics, MEMS, H-Temp, HV, imaging, smart cards
- New actors: Philips, Alcatel, Kopin, Gemplus, ST, etc

20% higher speed doubles the price of µP.
SOI offers more than 20% gain in speed....

SOI Products

- High Performance Logic :
  - \+ performance driven, no cost sensitive at leading edge
  - \+ technology driver, moderate volumes
  - \- long development, circuit complexity
- Embedded solution :
  - \+ performance, relative simplicity, die shrink
  - \- cost sensitive & large volumes in mass production
- Communication & Smart Cards :
  - \+ low power/voltage well matching SOI
  - \+ computational talent
  - \- cost sensitive

UNIBOND



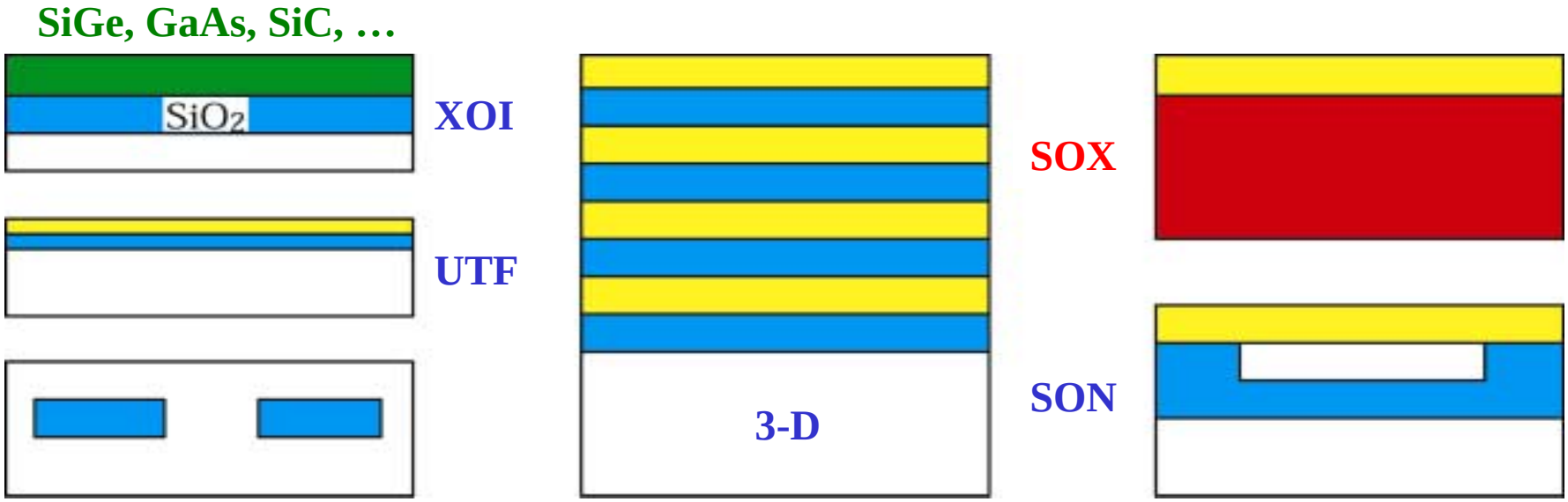
Smart Cut [Bruel '95]

- No etch-back needed
- Excellent crystal quality
- Thermal BOX
- High quality back interface
- Bonded interface below the BOX
- Film and BOX thickness adjustable
- High-grade active wafer recyclable
- Cheap support wafer: low cost
- Conventional equipment only
- High volumes

Eltran : wafer separation defined by a sacrificial layer of porous Si

The Horizon: New SOI-like Structures

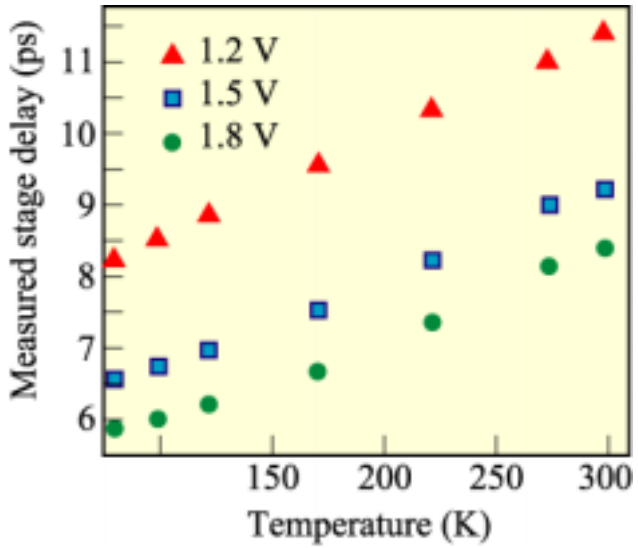
→ Novel devices with enhanced performance and functionality



SOI = Semiconductor On Insulator

Why is cold silicon cool ?

- Improved transport properties
  - higher mobility ($\mu \sim T^{-1.5}$) and saturation velocity (+ 50-100%)
  - velocity overshoot in ultra-short devices
- Better subthreshold swing (S ~T)
- Reduced leakage current ($I \sim e^{-E/kT}$)
- Reduced electromigration & interconnect resistance
- Possible combination CMOS + superconductors
- Lower thermal noise
- Improved thermal conductivity of silicon
- Ideal for quantum and single-electron devices
- Improved speed for cryogenic operation



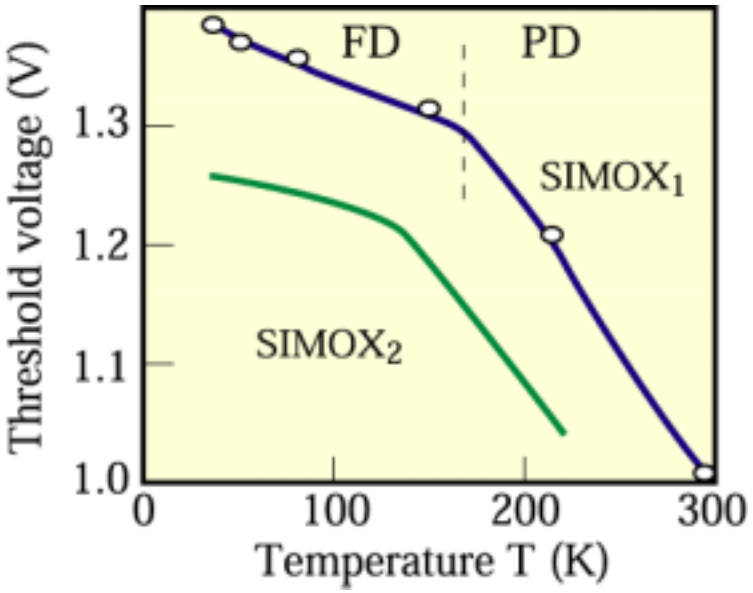
Performance oriented !!!

Threshold Voltage

At low T:

- Fermi level increases
- Threshold voltage increases
- Depletion depth extends
- Double slope: transition from partial to full depletion

dV_T/dT = 1.9 mV/K (PD, α = 1) or 0.6 mV/K (FD, α = 0)

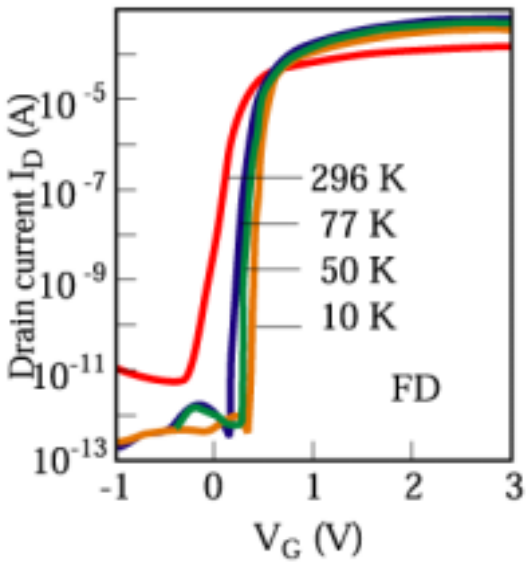


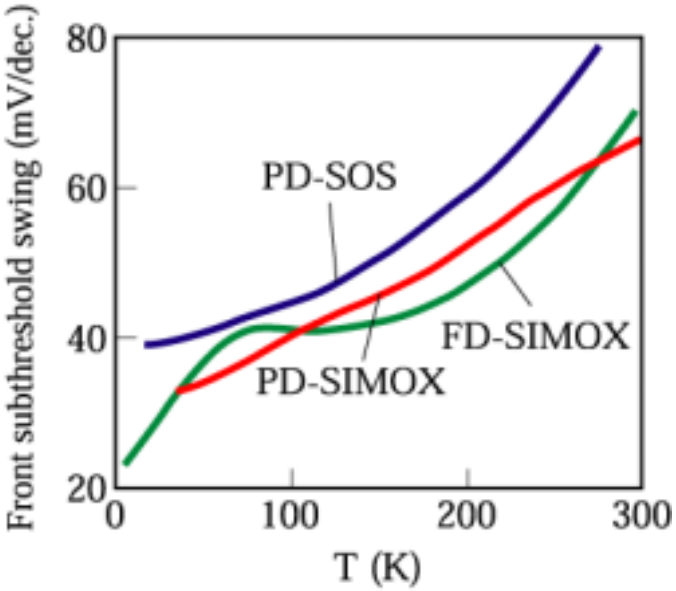
$$\frac{dV_T}{dT} = \frac{d\Phi_F}{dT} \times \left(\alpha \frac{C_D}{2C_{ox}} + \frac{qD_{it}}{C_{ox}} + 2 \right)$$

Subthreshold Swing

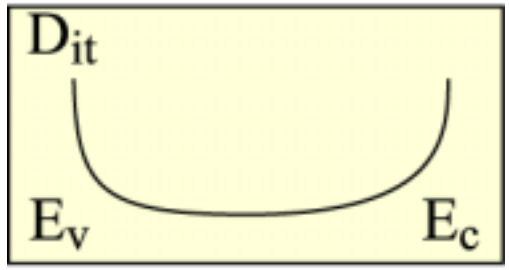
- Excellent swing (10-20 mV/decade) has been measured below 77 K
- The transition from partial to full depletion occurs at a lower T for the swing than for the threshold voltage
- The swing decreases quasi-linearly with temperature ...

  unless the density of front/back interface traps increases at low T



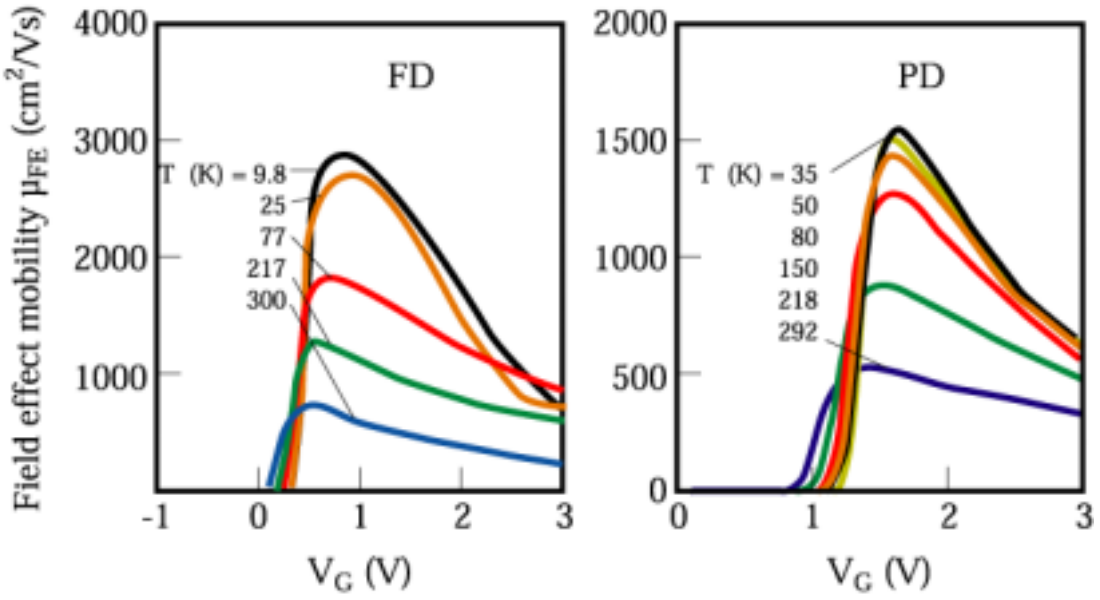


$$S = \frac{kT}{q}\left(1 + \frac{qD_{it1} + \alpha C_{si}}{C_{ox1}}\right)$$



Mobility in SOI MOSFETs

- High electron mobility (3000 cm^2/Vs) at low T
- Band splitting: higher mobility in the second subband
- Mobility degradation with V_G accentuated at low T
  - higher series resistance
  - larger coefficients $\theta_{1,2}$
  - possible negative transconductance

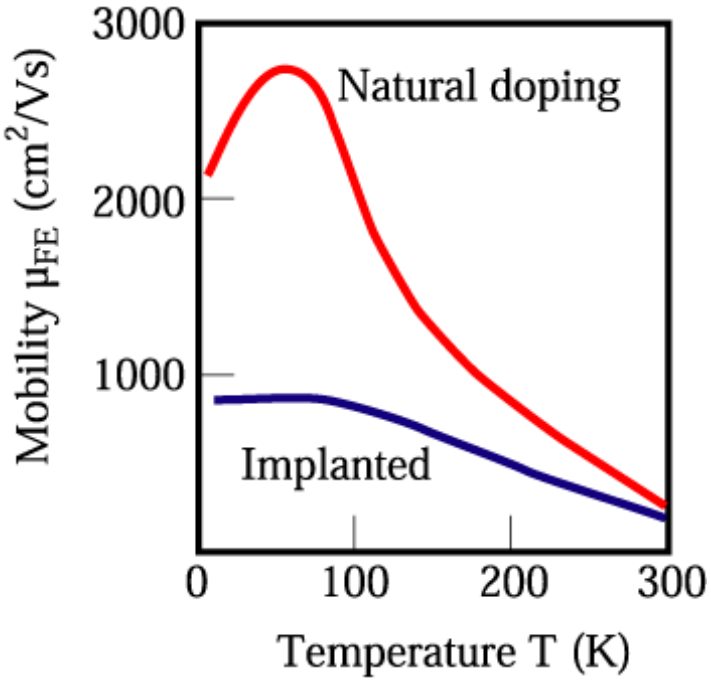


Low-T Mobility Laws

- **Scattering mechanisms**
  - ionized impurities (Coulomb) at low T: $\mu \sim T^{1.5} \times (Q_{inv})^{-1}$
  - phonons at high T: $\mu \sim T^{-n} \times (Q_{inv})^{-1/3}$
  - surface roughness: $\mu \sim T^{-1/3} \times (Q_{inv})^{-2}$
- **Bell-shaped variation**

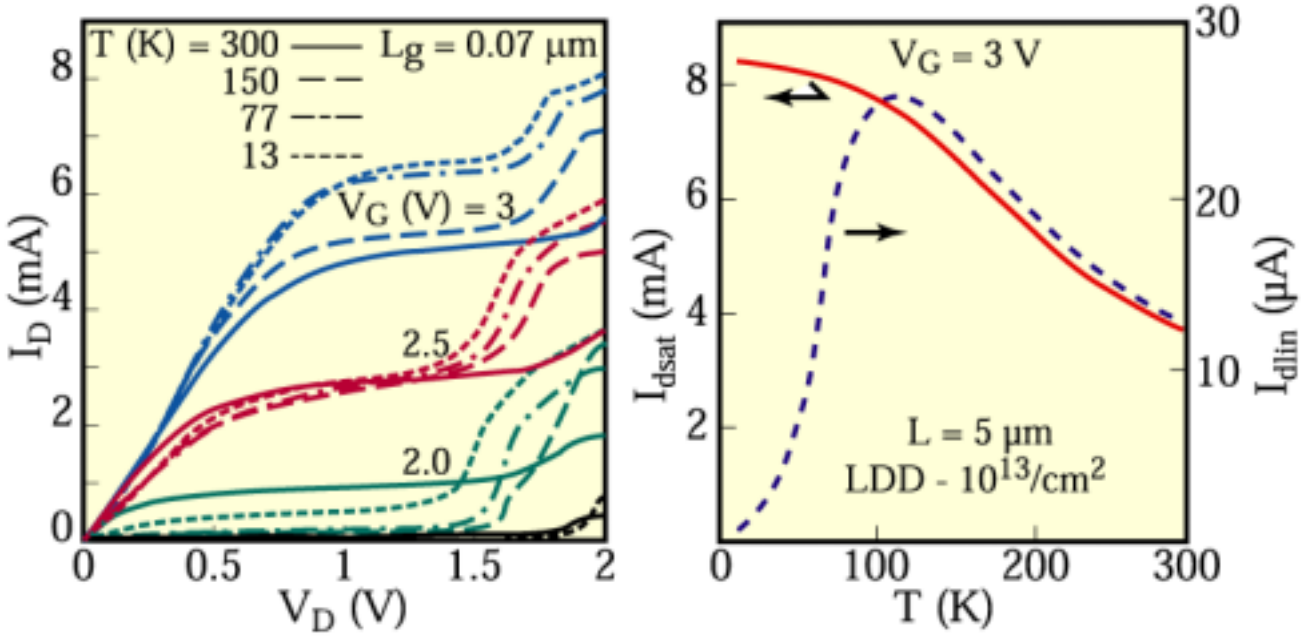
$$\mu_{eff} = \mu_0 \times \frac{(Q_{inv}/Q_c)^{n-2}}{1+(Q_{inv}/Q_c)^{n-1}}$$

- n = 3, for T < 77 K
- n = 2, for T > 77 K



Drive Current

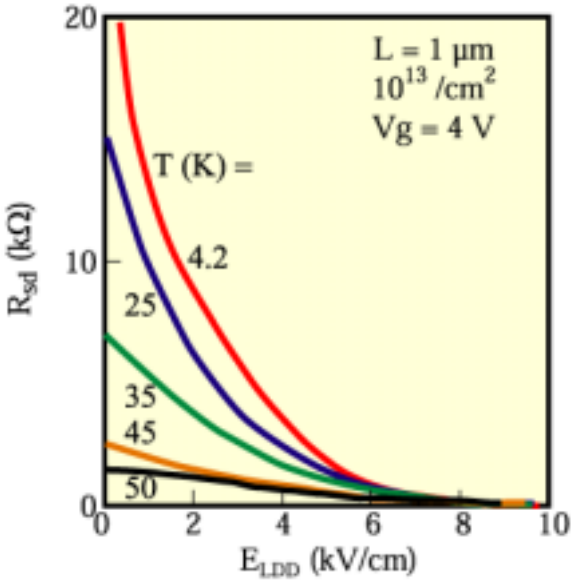
- Drain current can increase or decrease at low-T
- Impact of device architecture (inversion or accumulation mode, LDD, …)
- Competing mechanisms
  - mobility, threshold voltage, series resistance (all increasing at low-T)

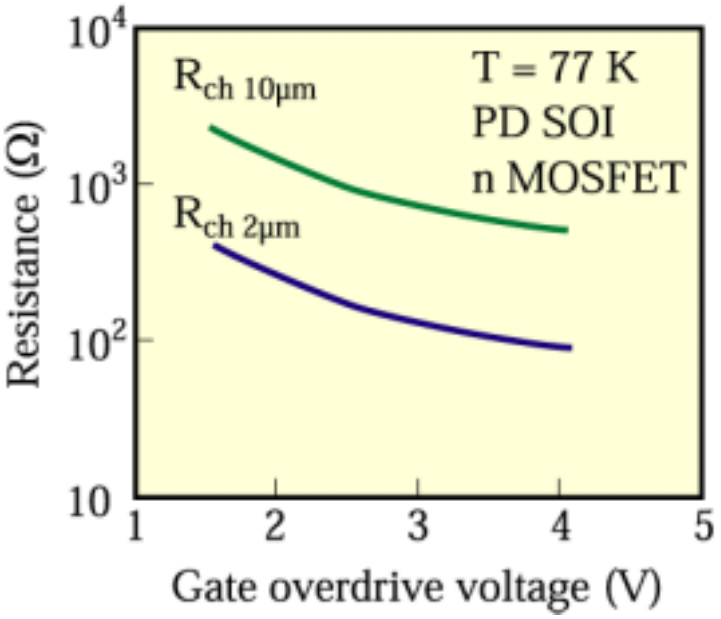


Series Resistance at Low-T

- R_{SD} increases for low T and low V_G
- Increasing V_G causes field-effect impurity ionization: $R_{SD} = f(V_G)$!!!
- Parameter extraction problems:

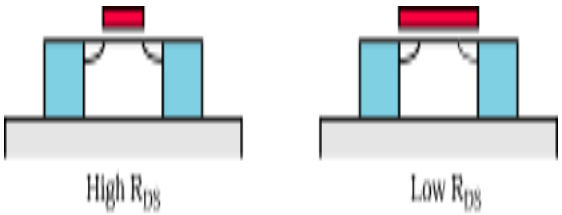
$$1/\mu \sim 1 + \theta_1(V_G - V_T) + \theta_2(V_G - V_T)^2, \text{ with } \theta_1 = \theta_0 + R_{SD}C_{OX}W/L$$





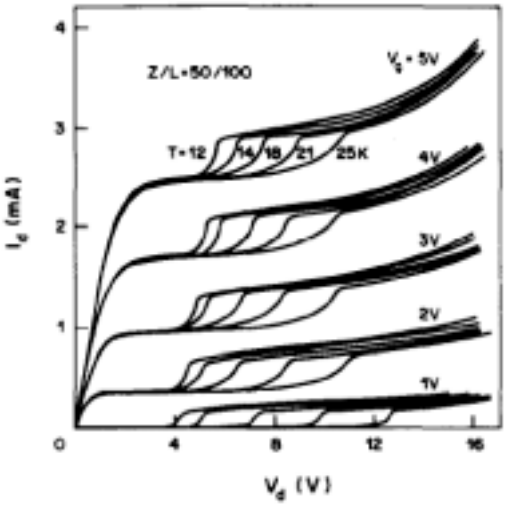
R_{SD} and θ depend on device architecture:

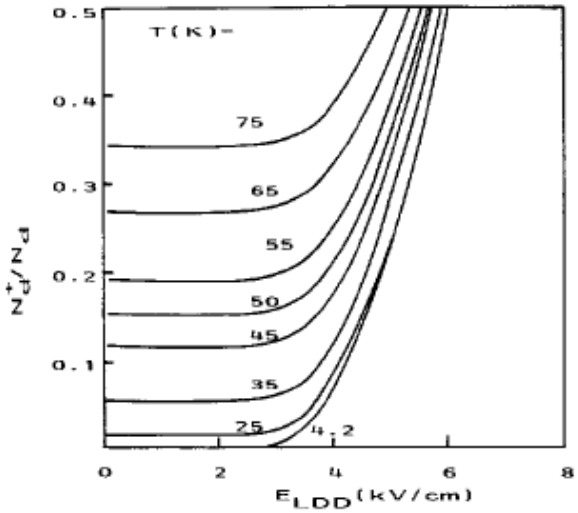
- LDD
- inversion or accum.
- gate overlap



Impurity Freeze-Out

- 77 K : weak freeze-out
  - R_{SD} increases $\Rightarrow$ LDD optimization
  - lateral field decreases $\Rightarrow$ less impact ionization
- 30 K : strong freeze-out
  - field-effect ionization (via V_G and V_D)
  - $I_D(V_G)$ curves may change according to V_D
- SOI-like kink even in bulk MOSFETs
- Fully-depleted SOI MOSFETs
  - naturally kink free
  - suppressed kink-related excess noise
- Forget about body contacts





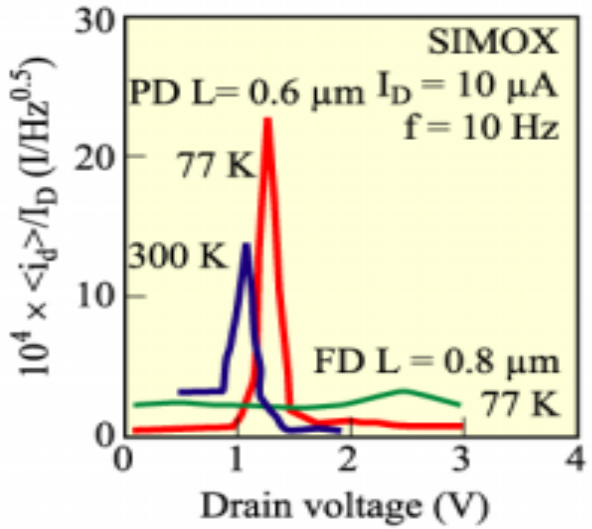
Special Effects in SOI MOSFETs at Low T

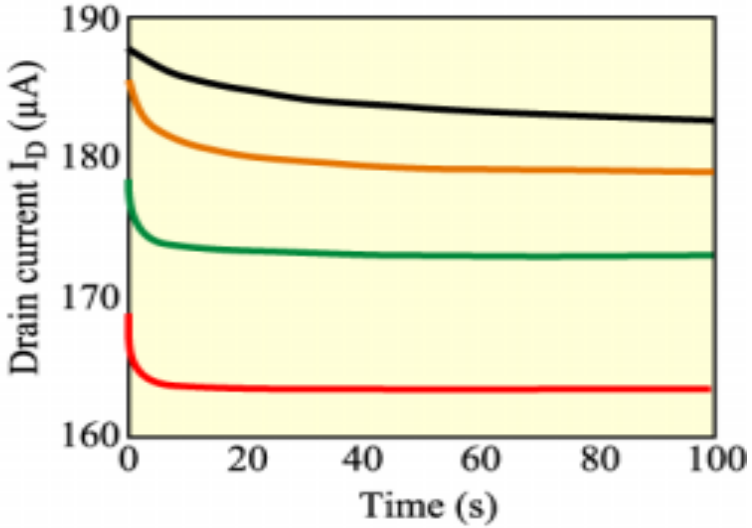
Noise:

- reduced thermal noise
- increased 1/f noise (higher D_{it})
- kink-related excess G-R noise

Transient & History Effects:

- longer transients:
  $\Delta t \sim \tau N_A/n_i$ (n_i decreases)
- history & frequency effects ???
  work needed





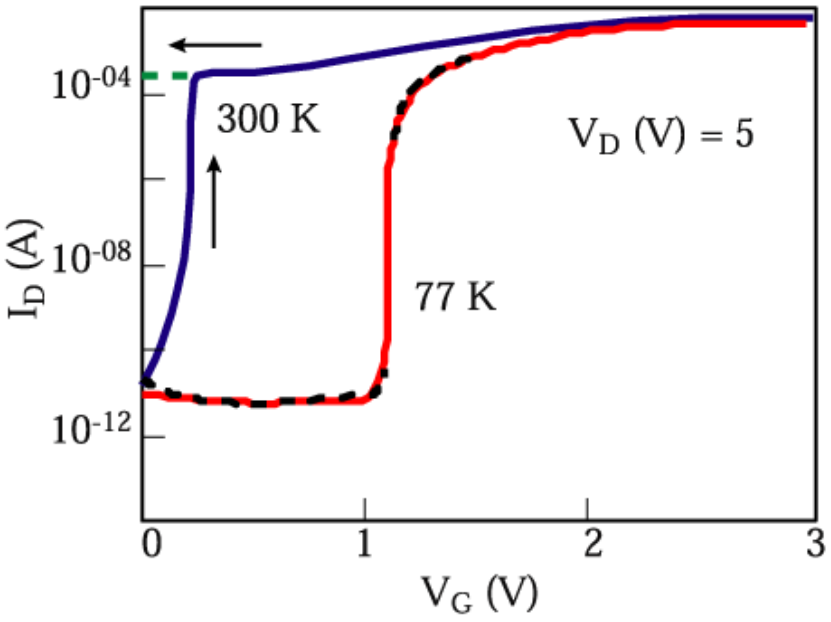
Short-Channel Effects in SOI MOSFETs

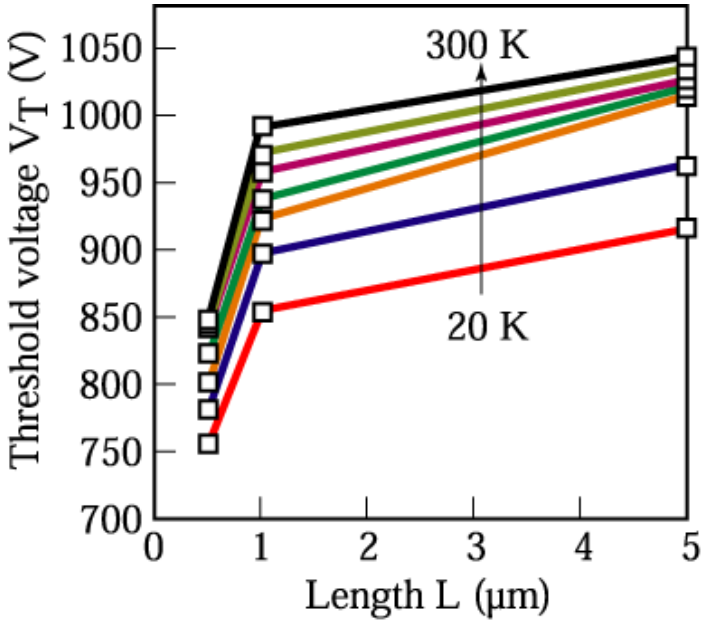
Charge sharing and DIBL:

- weak T-impact on $V_T(L)$: small variation of the depletion regions

Parasitic Bipolar Transistor:

- strongly attenuated: bipolar gain decreases at low T
- no latch at 77 K & higher breakdown voltage





Short-Channel Effects in SOI MOSFETs

Gate-Induced Drain Leakage (GIDL):

- due to carrier tunneling in the gate-drain overlap region
- base current amplified by bipolar gain
- reduced at low T
  - band-to-band tunneling & bipolar gain decrease

Reverse Short-Channel Effects:

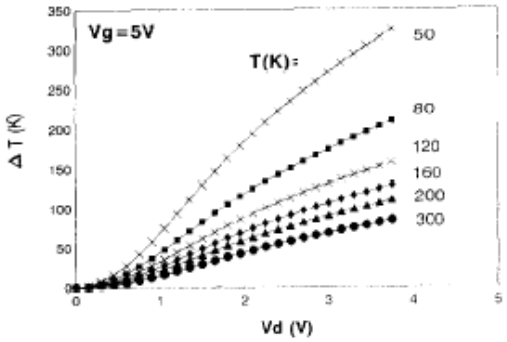
- due to doping inhomogeneity near S & D
- highly reduced at low T
  - doping effects erased by freeze-out

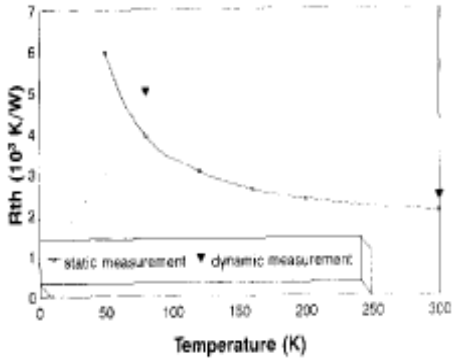
Hot-Carrier Degradation:

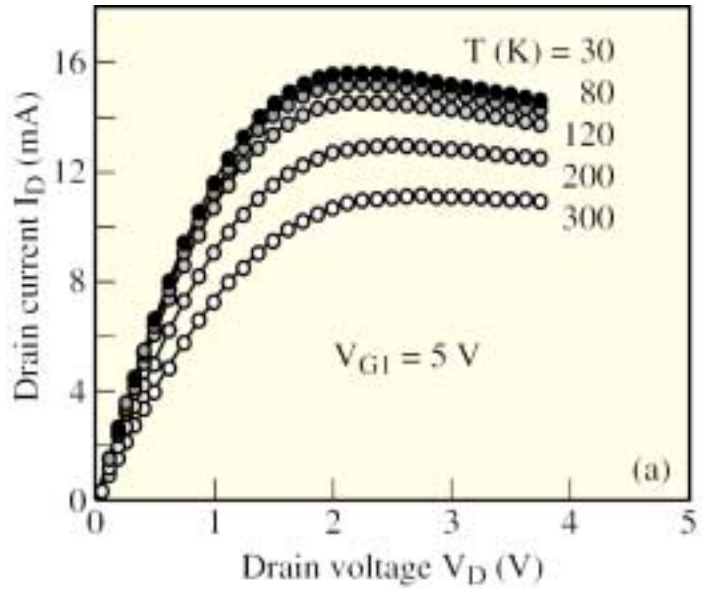
- more severe at low T
- complex mechanisms
  - reduced bipolar effect, increased V_T, more or less drain current
  - higher gate current, enhanced trapping, more impact ionization
  - in very short-channels: less impact ionization
    non-stationary transport: reduced field peak & pinch-off region

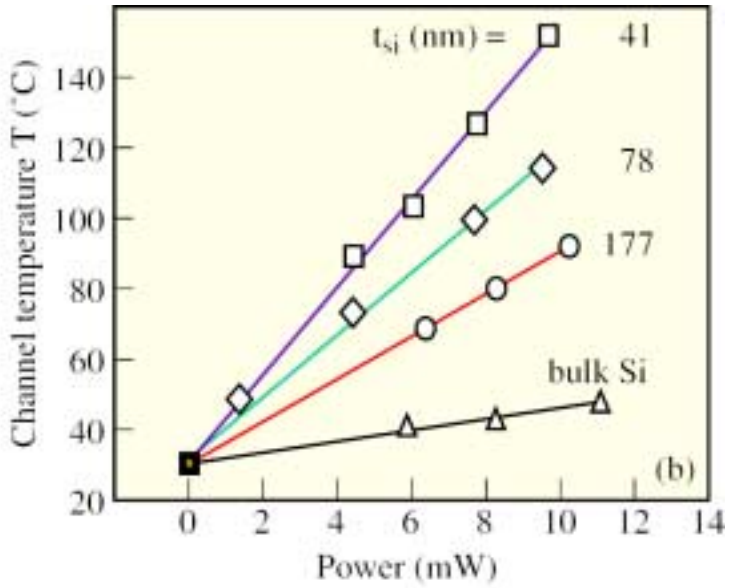
Self-Heating in SOI MOSFETs

- Self-heating: $\Delta T = R_{TH} I_D V_D$
- ΔT increases in thin films, thick BOX, and low T
- Both R_{TH} and I_D increase at low T









How to Reduce Self-Heating? Just Use I in SOI ...

- Replacement of BOX with thin buried alumina: R_{TH} is highly lowered
- ΔT reduced by 50 K !!!

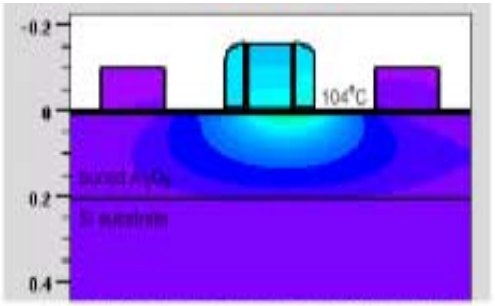


Fig. 7. 2-D temperature profiles in a SOI MOSFET with buried Al_2O_3 (Vg=Vd=2V).

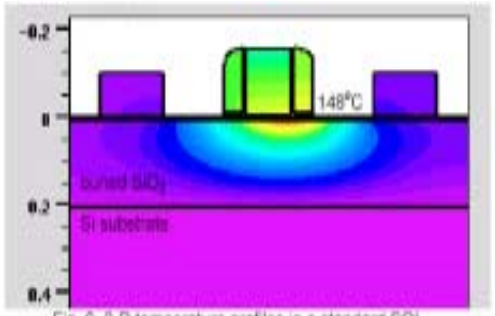
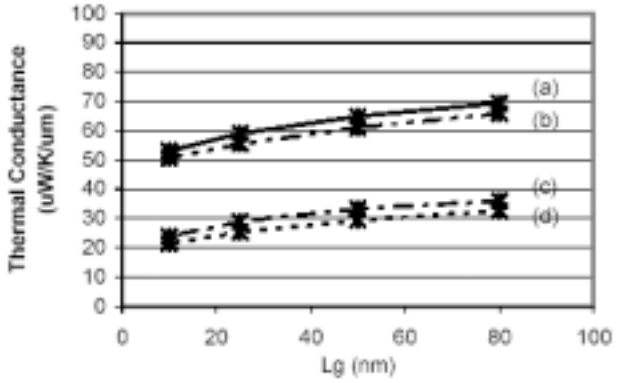
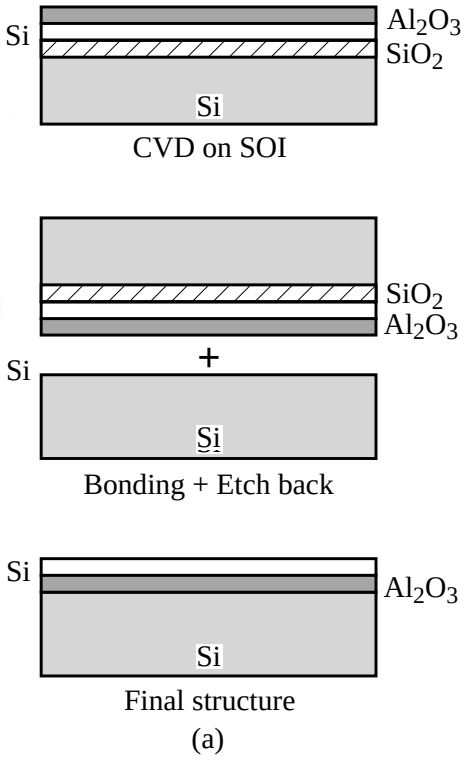
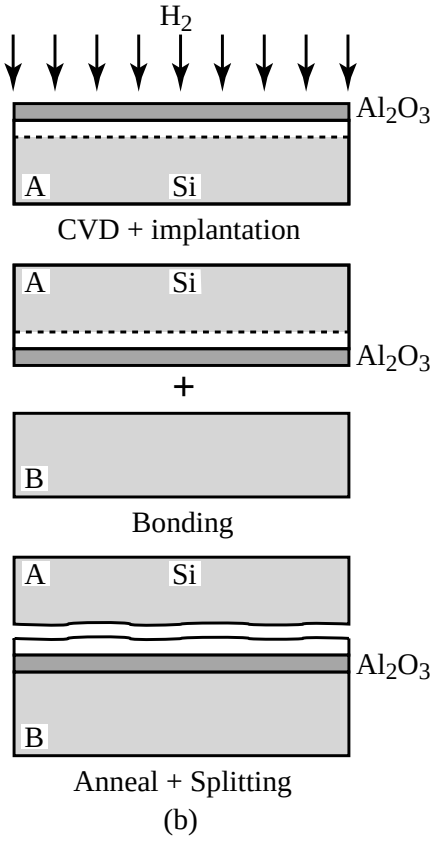


Fig. 8. 2-D temperature profiles in a standard SOI MOSFET with buried SiO_2 (Vg=Vd=2V).







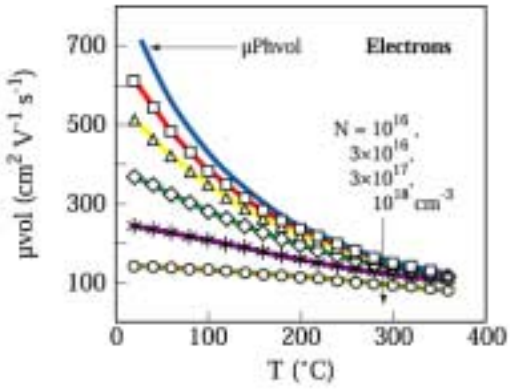
Why is SOI a HOT topic ?

- **High Temperature operation**
  - application oriented: oil industry, automobiles, aeronautics, ...
  - trade-off : market opening vs. still acceptable performance
  - bulk Si is very limited
  - high-T semiconductors (SiC, diamond,…) are not ready yet for volume production
  - High complexity IC's operate at increased T (self-heating)

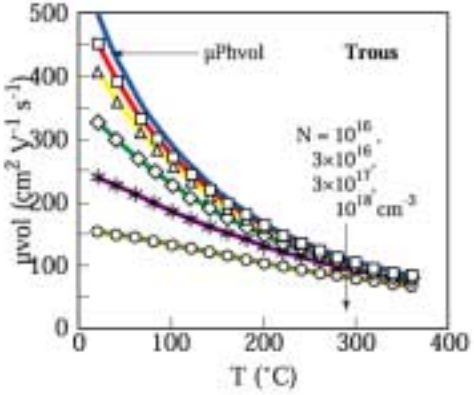
- **SOI has strong arguments**
  - reduced leakage current
  - attenuated threshold voltage shift
  - feasibility in the 300°C range

Si Parameters at High Temperature

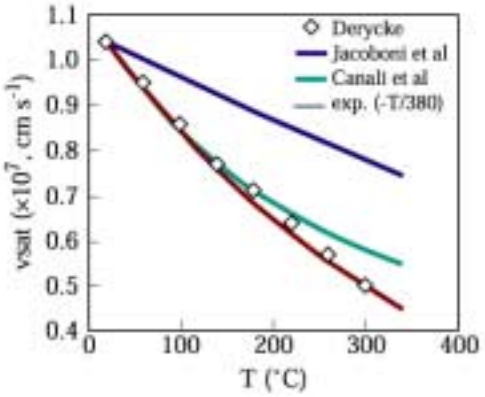
- Mobility and velocity saturation decreases: lower speed
- Higher density of states and intrinsic carrier density



Electron mobility



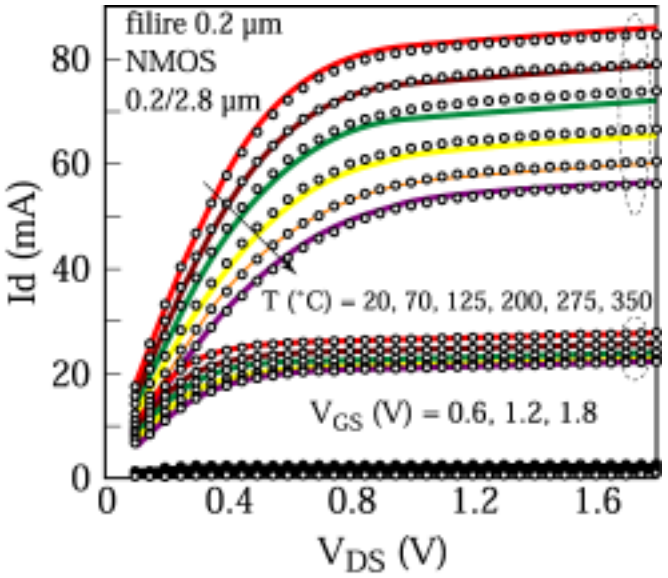
Hole mobility

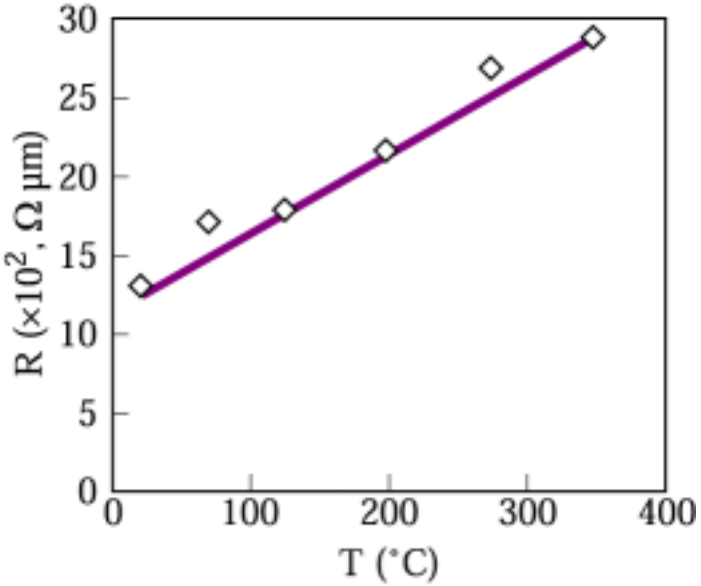


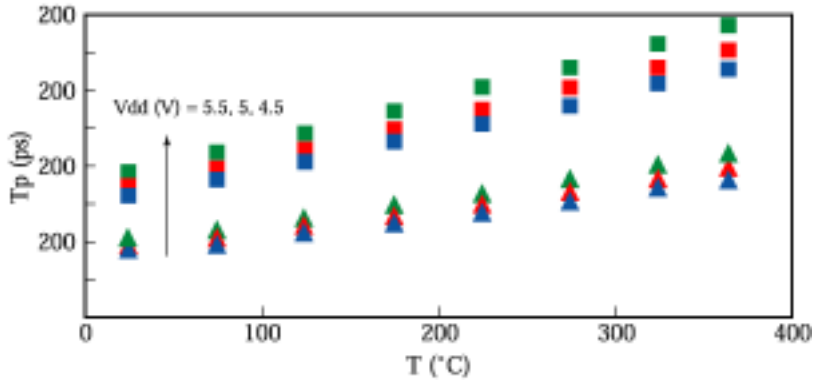
Saturation velocity (electrons)

Characteristics of SOI MOSFETs at High Temperature

- Reduced drain current
- Higher series resistance
- Degraded delay time in inverters

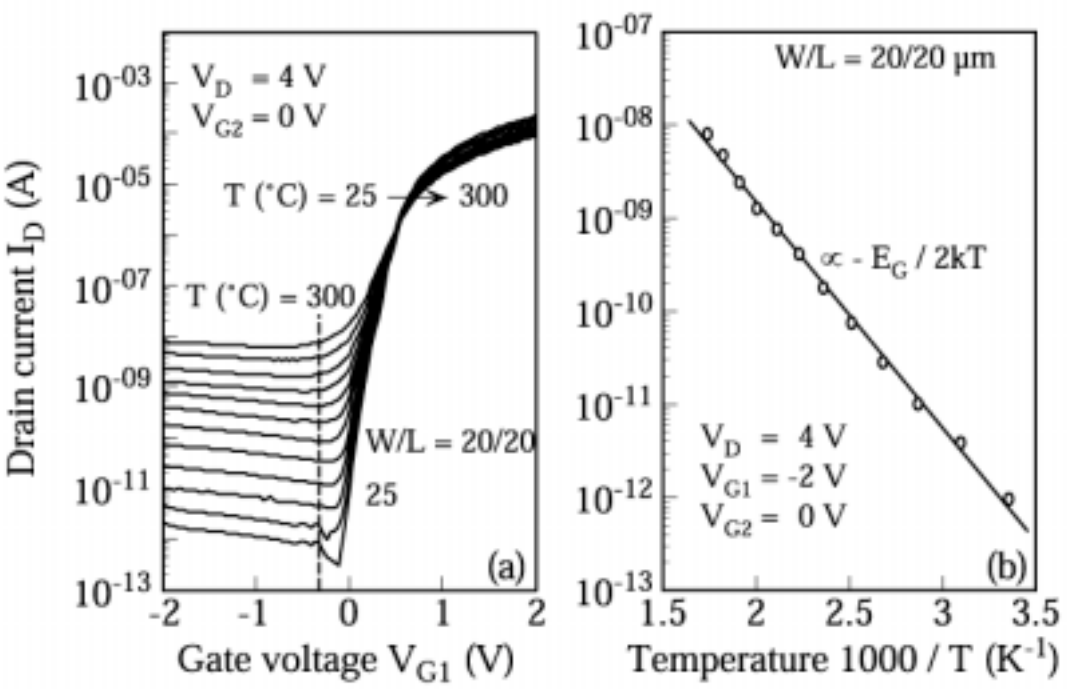






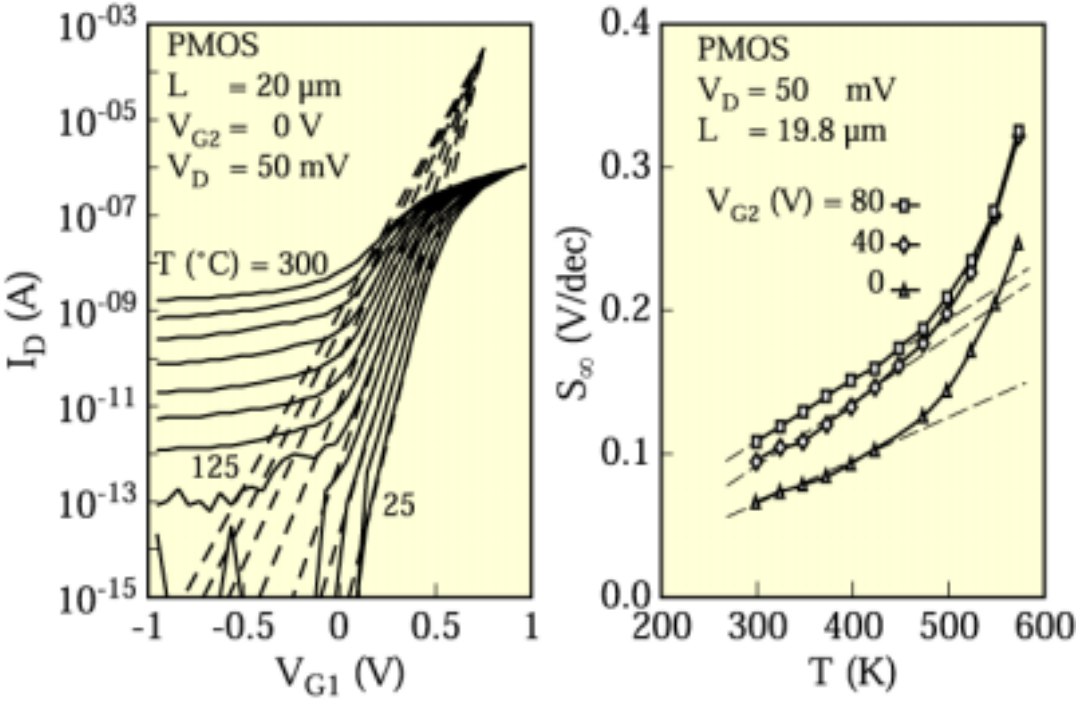
Leakage Current in SOI MOSFETs at High Temperature

- Leakage current increases exponentially ($E_A = E_G/2$)
- Still much lower than in bulk-Si
- For 300°C operation $I_{on}/I_{off} = 10^4$
- Wide temperature range



Subthreshold Characteristics of SOI MOSFETs at High Temperature

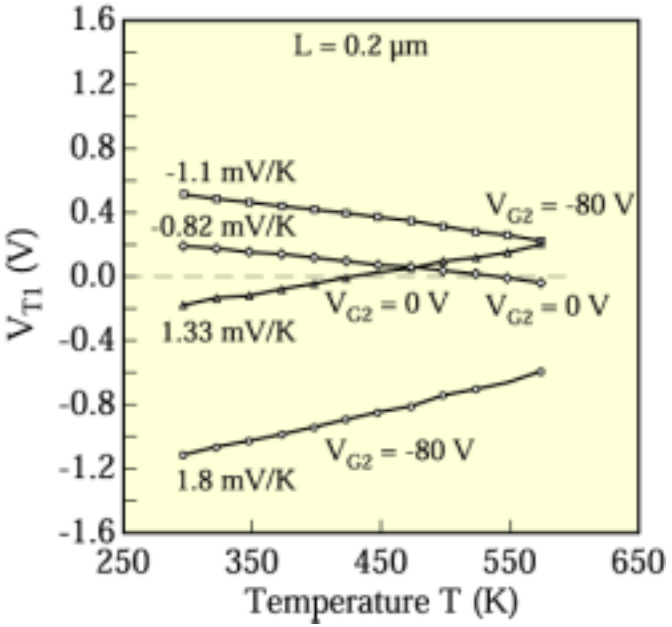
- Strong impact of leakage
- In Fully-Depleted MOSFETs
  - rather ideal swing S = 2.3 kT/q
- Above 200°C
  - swing exponentially increases with T, due to higher leakage

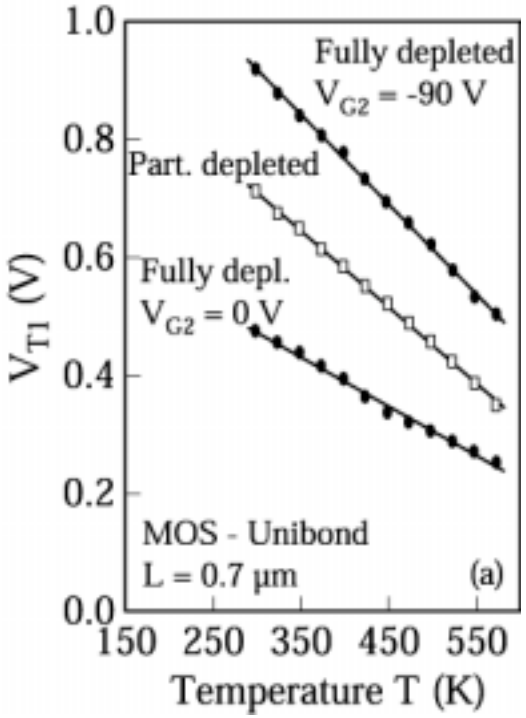


Threshold Voltage Reduction at High Temperature

- Fully depleted SOI outperforms partially depleted and bulk-Si MOSFETs

  $\Delta V_T / \Delta T$ = -0.5 mV/decade instead of 1.2-2 mV/decade
- Impact of film thickness, back-gate bias, and channel length
- Technology tunning: keep V_T large enough !



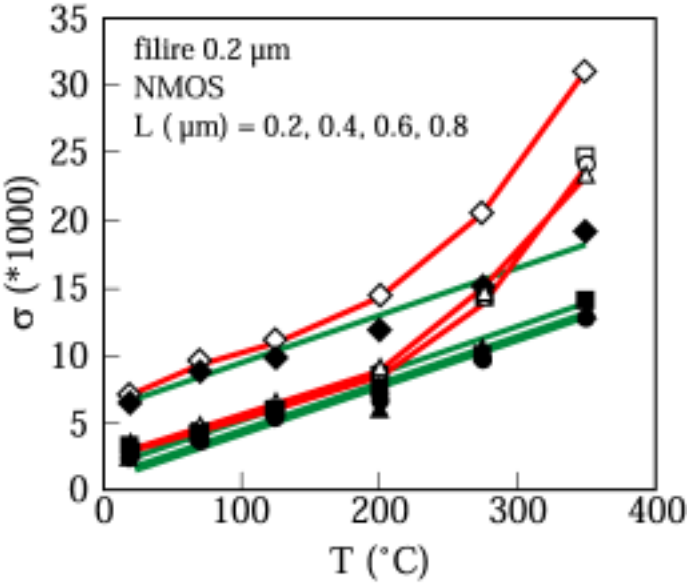


Short-Channel Effects in SOI MOSFETs at High Temperature

- Increased DIBL
(drain-induced barrier lowering)

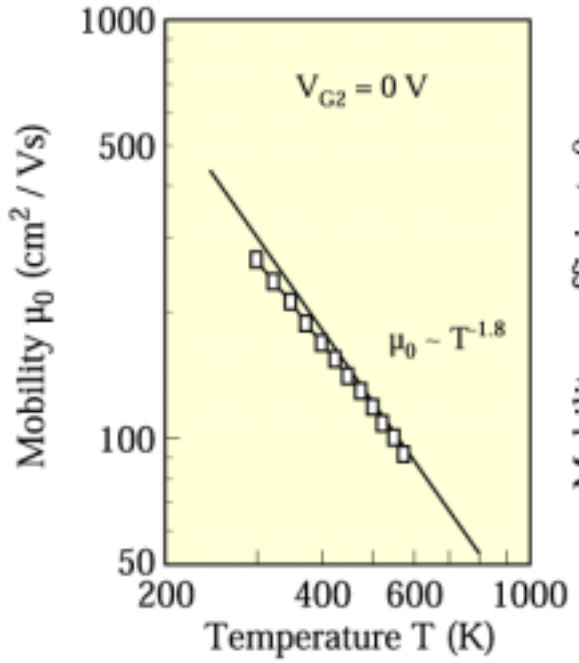
$$V_T(V_D) = V_T(0) - a\,V_D$$

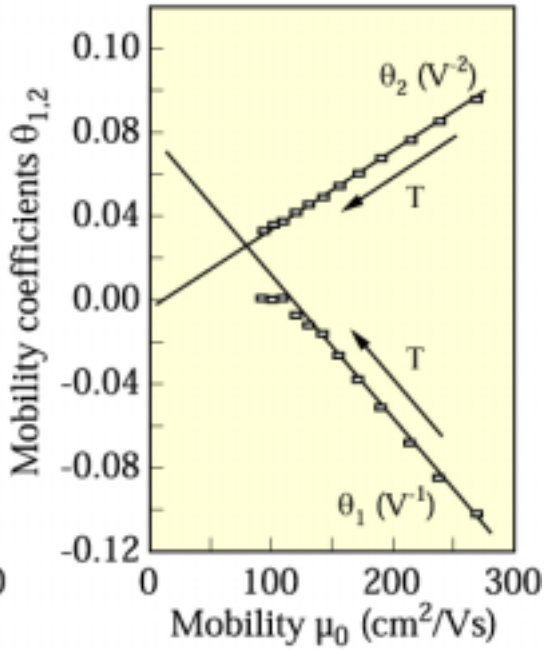
- DIBL coefficient a increases with T



Carrier Mobility in SOI MOSFETs at High Temperature

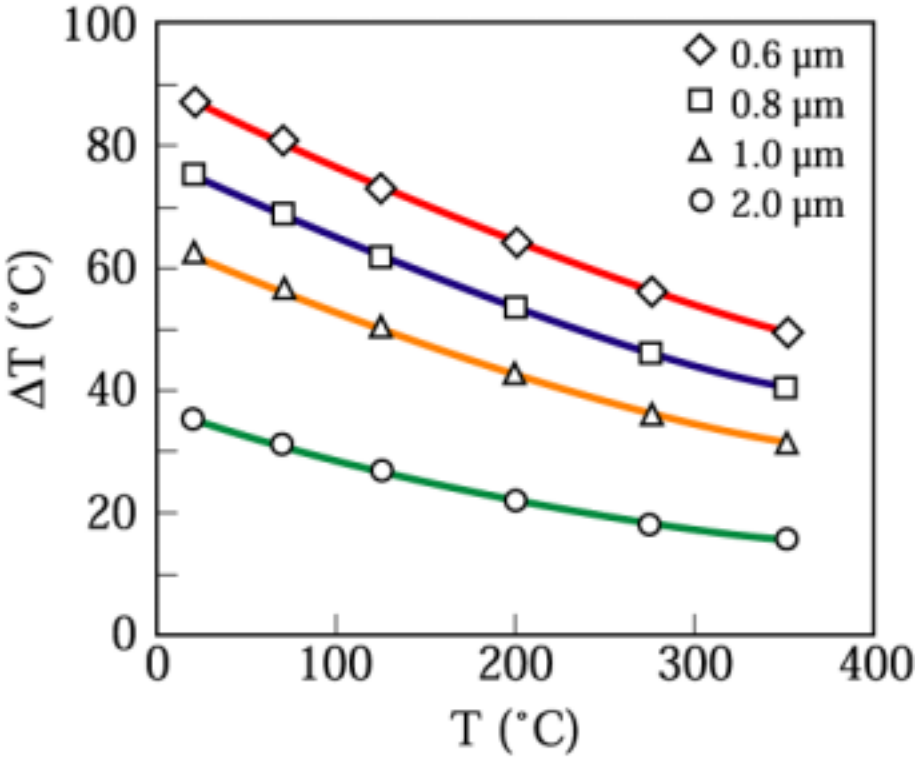
- **Low-field mobility: $\mu \propto T^{-1.8}$**
  - dominated by acoustic phonons
  - weak impact of doping and roughness
- **Mobility attenuation factors**
  - θ_1 depends on Rs
  - θ_2 depends on surface roughness
  - $\theta_{1,2}$ decrease at high T





Self-Heating in SOI MOSFETs at High Temperature

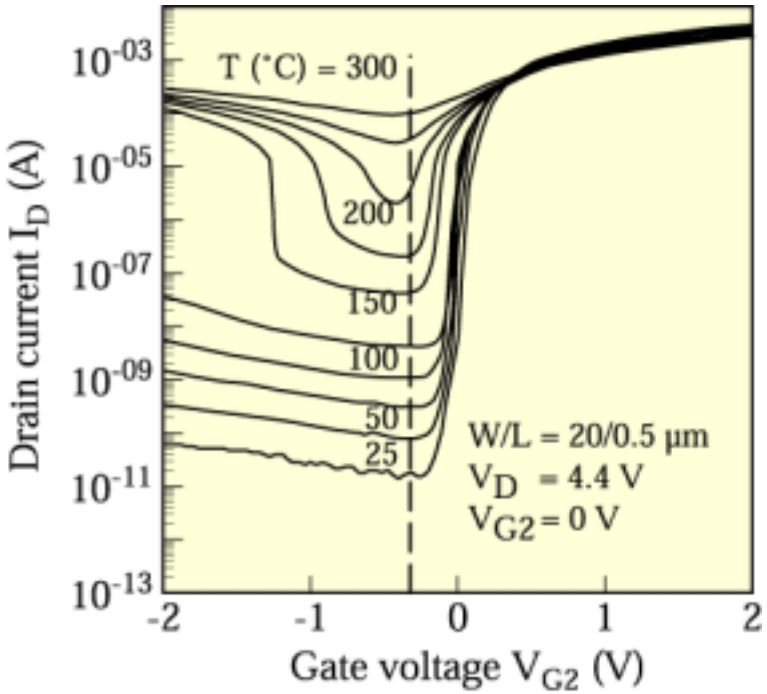
- Reduced self-heating
- Due to lower mobility and current

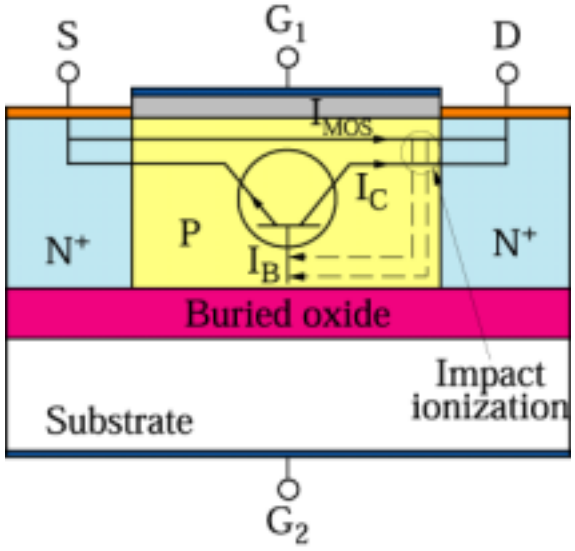


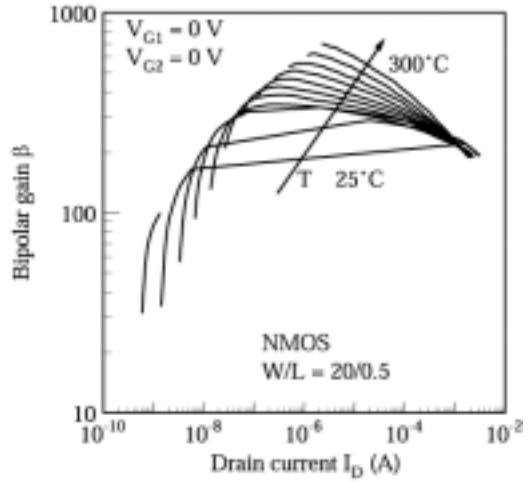
Measurement of the temperature rise in partially depleted SOI MOSFETs

Parasitic Bipolar Transistor at High T

- Increased bipolar action: gain β ↑↑ with T
- Attenuated impact ionization:
  carrier multiplication ↓ with T
- Latch occurs when T (or V_D) increases

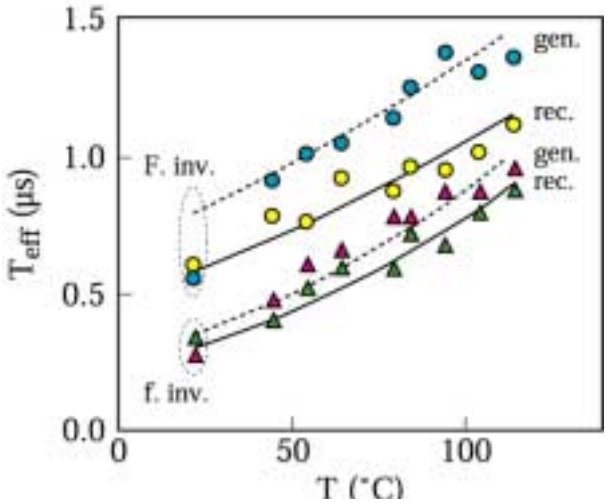


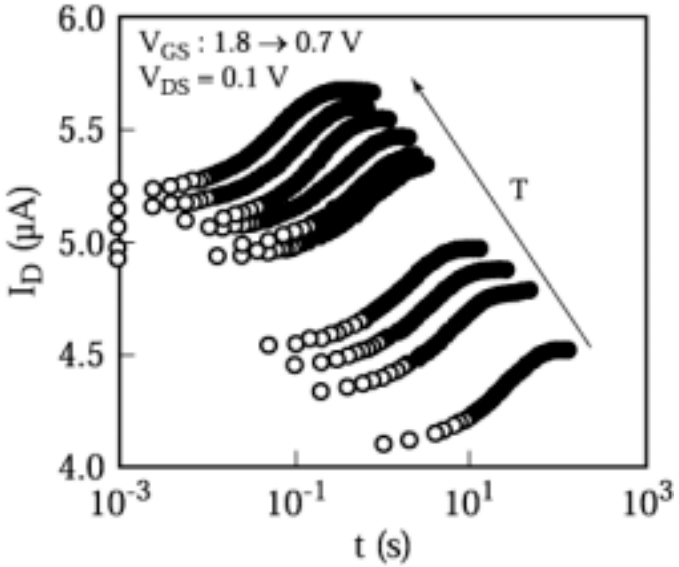


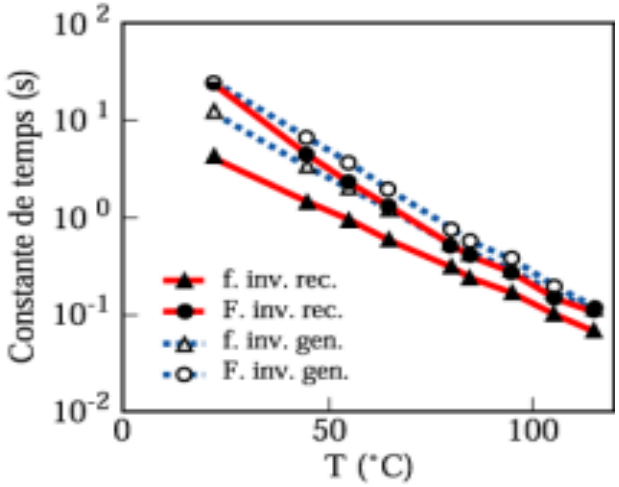


Transient Effects in SOI MOSFETs at High Temperature

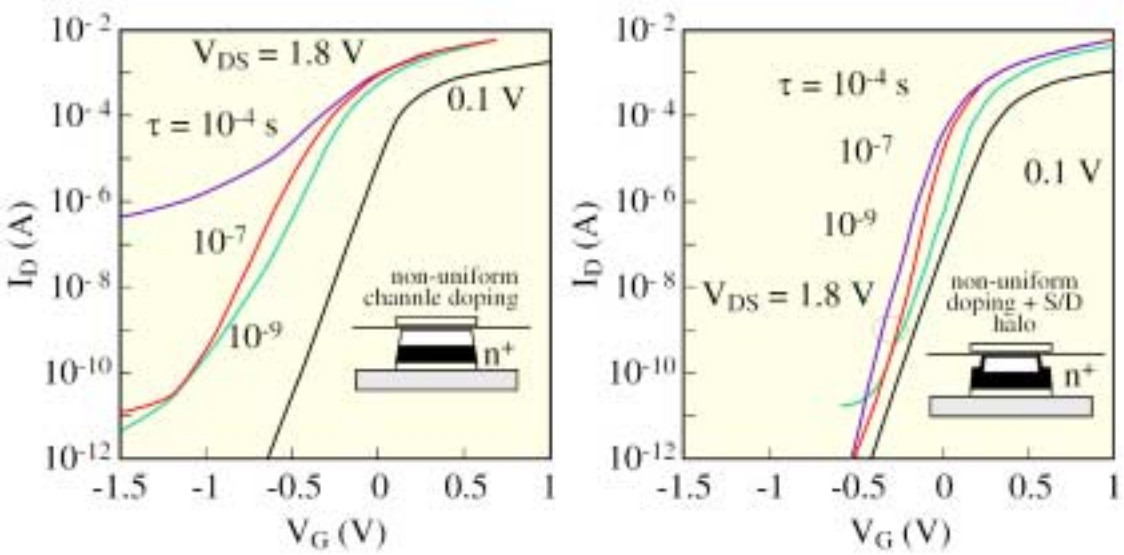
- Increased lifetime
- Smaller time constant
- Shorter transients
- Reduced history effects





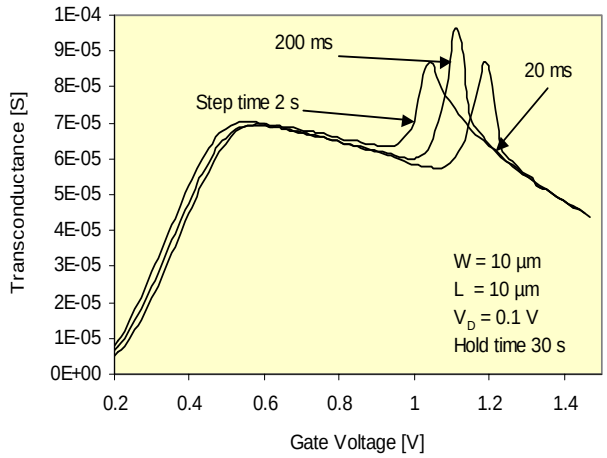


Floating-Body Effects in SOI MOSFETs



- FBE can be beneficial:
  - extra current
- Negative aspect:
  - subthreshold degradation
- How to suppress FBE ?
  - lifetime killing (unsuitable)
  - junction & halo engineering

[Shahidi '99]



⇐

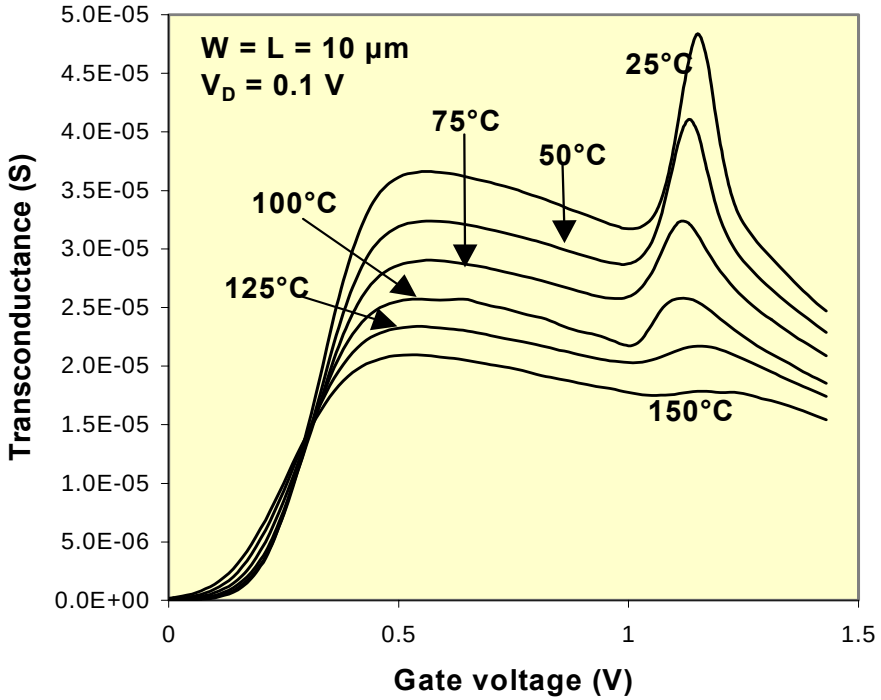
A new scaling-related effect:

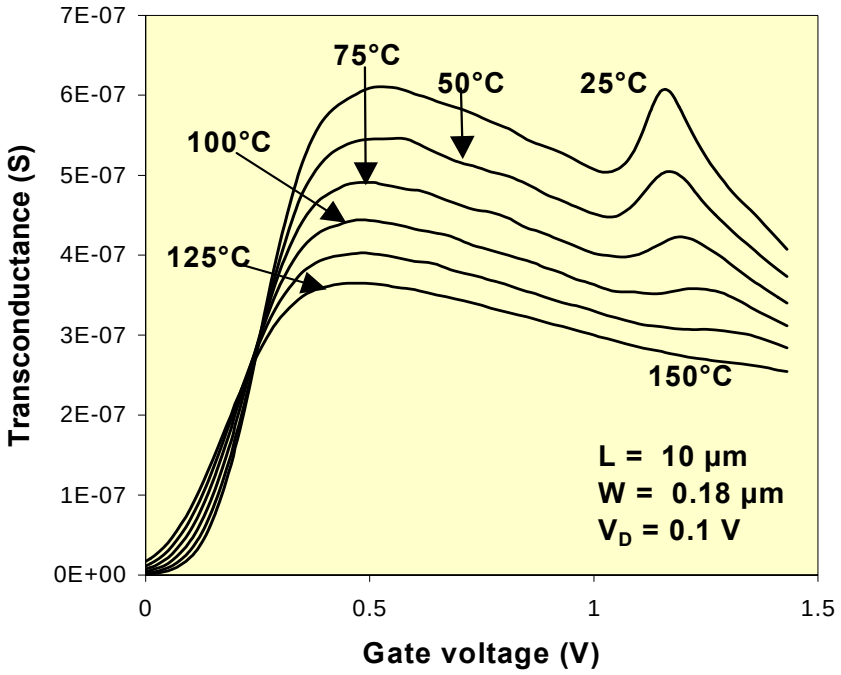
FBE induced by gate tunneling

- second peak in transconductance
- suppression of current transients (overshoot & undershoot)

[Pretet et al'02]

Reduction of Floating Body Effects at High T





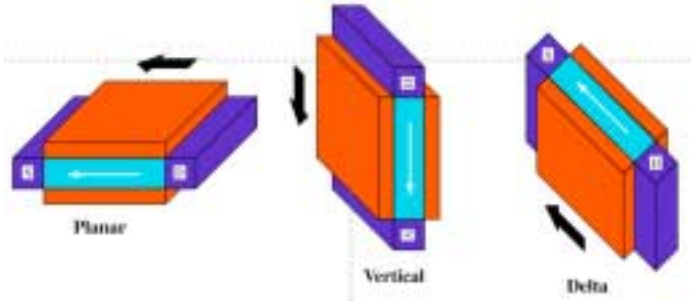
As T increases, the 2nd peak is reduced. Why ?

⇒ weak T-dependence of the direct gate tunneling current

⇒ strong increase of the junction recombination current

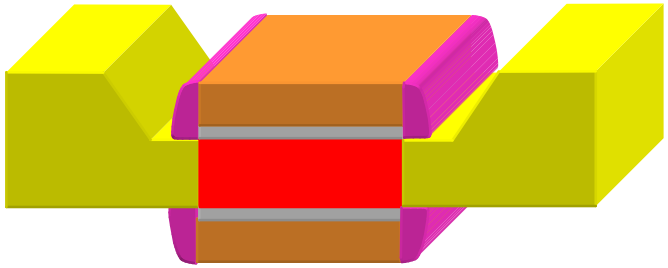
⇒ no junction engineering needed at high T

New Architectures: Double-Gate SOI MOSFETs



Why ?

- Excellent electrostatic control
- Best solution for ultimate scaling, down to sub-10 nm channel length
- Enhanced performance : current and transconductance



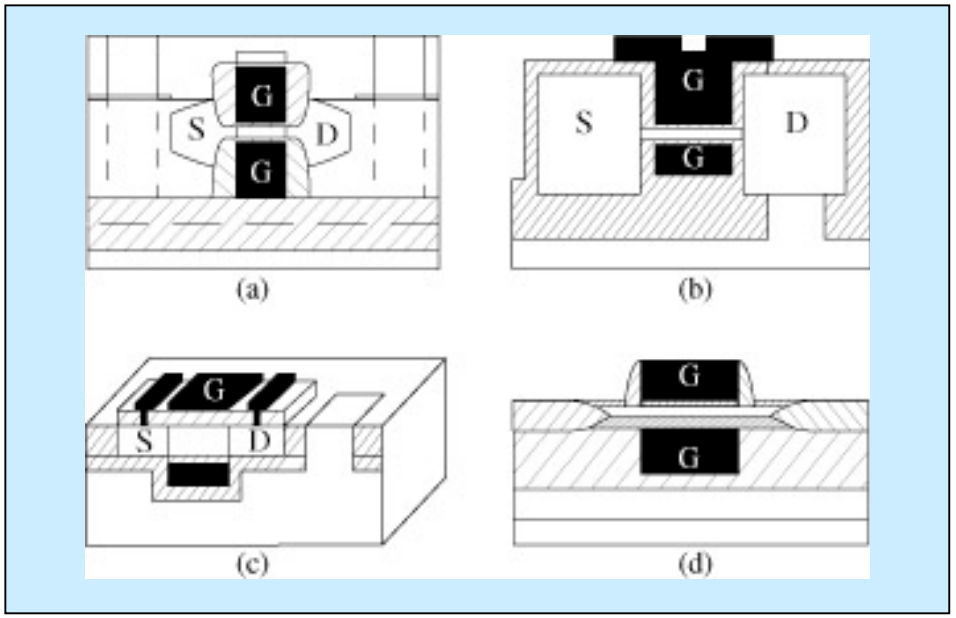
But:

Very difficult to process

Requirements:

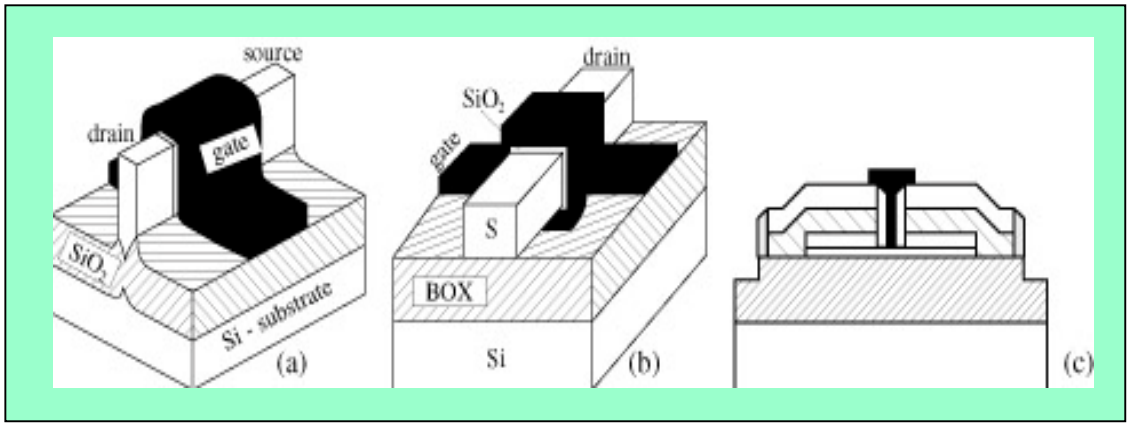
- ➢Variable width
- ➢Ultra-thin film ⇒ volume inversion
- ➢Uniform thickness
- ➢Low series resistance
- ➢Ultra-short channel
- ➢*Self-alignment of front / back gates ?*

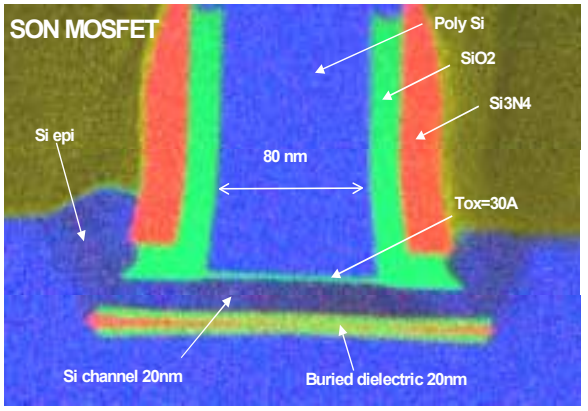
Double-Gate Structures



Technologies:

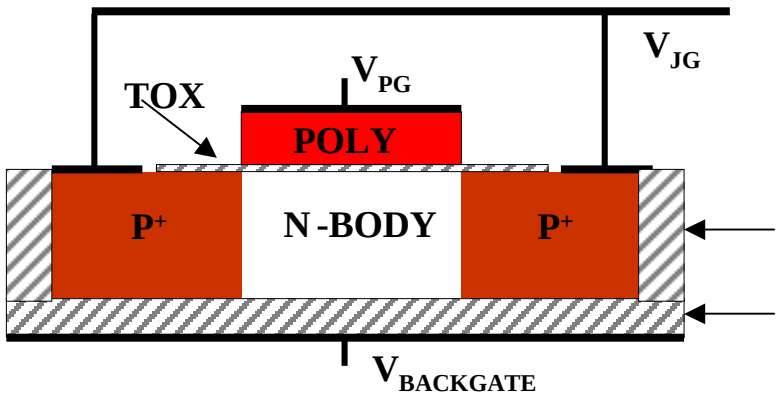
- gate stack
- tunnel epitaxy
- lateral epi growth
- bonding
- gate-all-around
- Delta
- Fin-gate
- SON



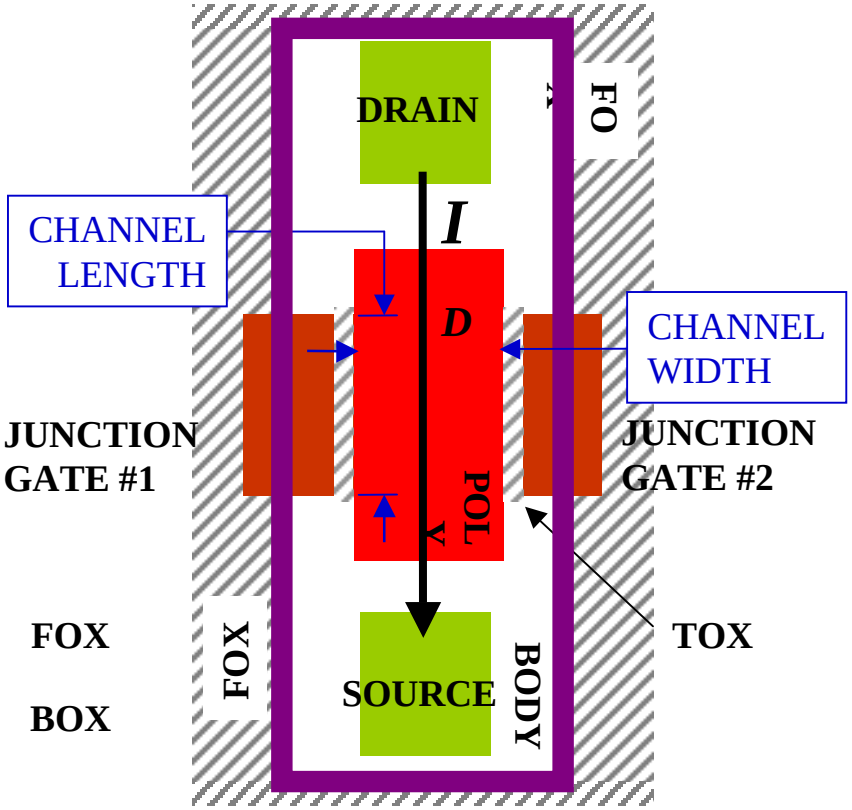


The 4-Gate Transistor : G⁴-MOSFET

- **A JPL revolutionary device !**
- **Maximum number of gates**
- **G⁴-MOSFET = MOSFET + JFET**
  - **2 lateral junction gates ⇒ JFET mode**
  - **Front and back gates ⇒ MOSFET mode**
- **Standard partially-depleted SOI technology**
- **Depletion/accumulation device**



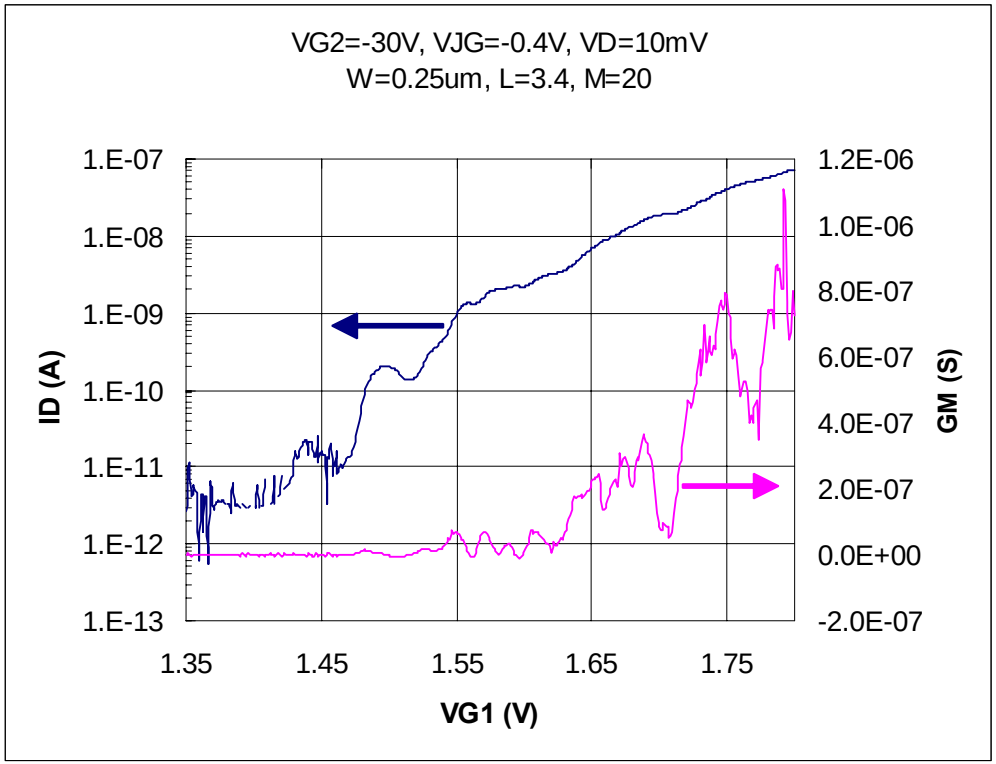
Cross-section view



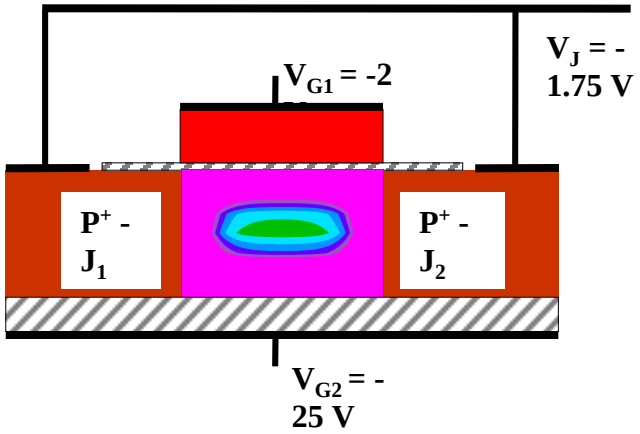
Arial View

G⁴-MOSFET: from Micro to Nano

- More negative bias on junction-gates ⇒ very narrow conductive wire
- All gates in depletion: conduction away from interfaces
  ⇒ high mobility, low noise, immunity to radiations



Electrically controlled quantum wire
⇒ size & position



Conclusions

- Low T operation of SOI MOSFETs : performance oriented
  - improved mobility, swing, speed
- High T operation : application oriented
  - SOI outperforms bulk-Si CMOS
  - lower leakage and Vt shift
  - SOI is needed !!
- Innovative devices are expected to operate better at low T
- Many aspects are still unclear at both low & high T
  - further studies necessary
  - device optimization adapted to the range of temperatures
  - appropriate design